IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method of forming metal wiring in a semiconductor device comprising:

forming a bottom metal pattern on a semiconductor substrate;

forming a low temperature oxide as an insulating layer on the semiconductor substrate including the bottom metal pattern, wherein the oxide is formed at the temperature of 150~500 C°;

forming a first photoresist pattern for forming via hole on the low temperature oxide ~~insulating layer~~;

forming an unfinished via hole by removing the low temperature oxide ~~insulating layer~~ selectively for a prescribed thickness using the first photoresist pattern as a mask, wherein a thickness of the low temperature oxide remaining inside the via hole is equal to or less than a thickness of an upper part of a damascene contact;

removing the first photoresist pattern;

forming a second photoresist pattern for forming a damascene pattern on the low temperature oxide ~~insulating layer~~ around the unfinished via hole;

forming a damascene pattern by removing the low temperature oxide ~~insulating layer~~ selectively using the second photoresist pattern as a mask;

removing the second photoresist pattern; and

forming a metal wiring via damascene contact by filling metal in the damascene pattern.

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Original) The method of claim 1, wherein the damascene contact is made of Cu, Al, W, Pt, Co, Ni, or alloy thereof.

6. (Currently Amended) The method of claim 1, wherein the damascene contact is formed by depositing metal on the low temperature oxide ~~insulating layer~~ including the damascene pattern and planarizing the metal by CMP process.

7. (Original) The method of claim 6, wherein the metal is deposited by electro-chemical deposition or dry deposition.

8. (Original) The method of claim 1, wherein the low temperature oxide is formed to have a thickness of 1,000~20,000Å.